L Number	Hits	Search Text	DB	Time stamp
1	2108	InAs or (indium adj arsenide) and (ohmic adj contact)	USPAT; US-PGPUB	2002/10/21 14:12
2	135	((InAs or (indium adj arsenide)) with substrate) and (ohmic adj contact)	USPAT; US-PGPUB	2002/10/21 14:12
4	34	(((InAs or (indium adj arsenide)) with substrate) and (ohmic adj contact)) and (Ti or Ni)	USPAT; US-PGPUB	2002/10/21 13:22
5	33	((((InAs or (indium adj arsenide)) with substrate) and (ohmic adj contact)) and (Ti or Ni)) and @ad<=20000928	USPAT; US-PGPUB	2002/10/21 13:22
6	1001	InAs or (indium adj arsenide) and (ohmic adj contact)	EPO; JPO; DERWENT; IBM_TDB	2002/10/21 14:12
7	24	((InAs or (indium adj arsenide)) with substrate) and (ohmic adj contact)	EPO; JPO; DERWENT; IBM_TDB	2002/10/21 14:13

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TITLE: Multi-layered structure for ohmic electrode fabrication

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An ohmic electrode for III-V compound semiconductors such as GaAs
semiconductors which has practically satisfactory characteristics is disclosed.
A non-single crystal **InAs** layer, **Ni** film, WSi film and W film are sequentially
deposited on an n.sup.+ -type GaAs **substrate** by sputtering, etc. and
subsequently patterned by lift-off, etc. to make a multi-layered structure for
fabricating ohmic electrodes. The structure is then annealed first at, e.g.
300.degree. C. for 30 minutes and next at, e.g.
650.degree. C. for one second
to fabricate an ohmic electrode.

At present, the most frequently used material of ohmic electrodes for GaAs
semiconductors is AuGe/Ni. The use of AuGe/Ni as the material of ohmic
electrodes makes it possible to fabricate ohmic electrodes in **ohmic contact**
with GaAs semiconductors by annealing at 400 to 500.degree. C.

Studies have so far been made on various materials for ohmic electrodes to
overcome these problems. The most ideal approach from the viewpoint of **ohmic**
contact is to establish **ohmic contact** by using metal which lowers the energy
barrier at the interface with an electrode metal and does not contain a
compound with a low melting point, such as .beta.-AuGa, as

shown in FIG. 2 in which EC is bottom energy of the conduction band, Ev is top energy of the valence band, and EF is the Fermi energy. This structure of ohmic electrode is obtained by epitaxially growing an In.sub.x Ga.sub.1-x As layer as an intermediate layer with a low energy barrier on a GaAs substrate by a metallorganic chemical vapor deposition (MOCVD) method, for example, and by providing an electrode metal on the layer. However, the use of an epitaxial growth equipment, such as MOCVD apparatus, to make the structure of ohmic electrode reduces the process window and degrades the mass productivity.

There is a report, directed to solution of these problems, which proposes to make on a GaAs **substrate** a multi-layered structure, such as InAs/W, InAs/Ni/W, Ni/InAs/Ni/W, and so forth, by depositing the intermediate **InAs** layer with a low energy barrier by a sputtering method using **InAs** as the target and by depositing the W and **Ni** films by an electron beam evaporation method and to apply subsequent annealing, which is said to result in obtaining an ohmic electrode having a good thermal stability (J. Appl. Phys. 68. 2475(1990)). FIG. 3 shows one of such examples in which the ohmic electrode is fabricated by depositing an **InAs** layer 201 on an n-type GaAs **substrate** 200 by a sputtering method, then depositing a **Ni** film 202 and a W film 203 sequentially on the **InAs** layer 201, and later annealing the structure.

A metal film, such as **Ni** film, may be provided between the III-V compound semiconductor body and the non-single crystal semiconductor layer for the purpose, among others, of improving the affinity of the non-single crystal semiconductor layer to the III-V compound semiconductor

body. The metal film may include an impurity behaving as a donor for the non-single crystal semiconductor layer.

In one embodiment of the ohmic electrode fabricating method according to the invention, the film on the non-single crystal semiconductor layer comprises a metal film and a refractory metal silicide film provided on the metal film. In this case, the metal film is used for the purpose, among others, of annealing at a lower temperature to make an ohmic electrode with a low contact resistance. The refractory metal silicide film is used as an impurity diffusion source for diffusing Si contained therein into the non-single crystal semiconductor layer as an impurity behaving as a donor for the non-single crystal semiconductor layer and also for the purpose of preventing elements constituting the non-single crystal semiconductor layer, e.g. In, from diffusing toward the electrode surface during annealing. For one or other reasons, such as reducing the sheet resistance of the ohmic electrode or permitting metal wiring to be connected to the ohmic electrode without the need for a barrier metal, there is preferably provided, on the refractory metal silicide film, a refractory metal film having a lower resistivity than that of the refractory metal silicide film and unlikely to react on a material used for wiring. The metal film may be a **Ni** film or a Co film. The refractory metal silicide film may be a WSi film, or other film such as MoSi film, TaSi film, and so on. The refractory metal film may be a W film, or other film such as Mo film, Ta film, and so on.

In another embodiment of the ohmic electrode fabricating method according to

the invention, the film on the non-single crystal semiconductor layer comprises a metal film containing an impurity behaving as a donor at least for the non-single crystal semiconductor layer and a refractory metal film provided on the metal film. In this case, the metal film containing an impurity behaving as a donor at least for the non-single crystal semiconductor layer is used for the purpose of annealing at a lower temperature so as to make an ohmic electrode with a low contact resistance and for making it behaves as an impurity diffusion source for diffusing in the non-single crystal semiconductor layer an impurity behaving as a donor therefor. The refractory metal film is used for the purposes, among others, of reducing the sheet resistance of the ohmic electrode and permitting metal wiring to be connected to the ohmic electrode without the need for a barrier metal. The metal film may be a **Ni** film or a Co film. The refractory metal film may be a W film, or other film such as Mo film, Ta film, and so on.

In another embodiment of the ohmic electrode fabricating method according to the invention, the film on the non-single crystal semiconductor layer comprises a metal film, a film comprising an impurity behaving as a donor at least for the non-single crystal semiconductor layer and a refractory metal film provided on this film. In this case, the metal film is used for the purpose, among others, of annealing at a lower temperature so as to make an ohmic electrode with a low contact resistance. The film comprising an impurity behaving as a donor at least for the non-single crystal semiconductor layer is used as an impurity diffusion source for diffusing in the non-single crystal semiconductor layer an impurity behaving as a donor therefor. The

refractory metal film is used for the purposes, among others, of reducing the sheet resistance of the ohmic electrode and permitting metal wiring to be connected to the ohmic electrode without the need for a barrier metal. The metal film may be a **Ni** film or a Co film. The refractory metal film may be a W film, or other film such as Mo film, Ta film, and so on.

In another embodiment of the ohmic electrode fabricating method according to the invention, the non-single crystal semiconductor layer contains an impurity behaving as a donor at least for itself, and the film on the non-single crystal semiconductor layer comprises a metal film and a refractory metal film provided thereon. In this case, the metal film is used for the purpose, among others, of annealing at a lower temperature so as to make an ohmic electrode with a low contact resistance. The refractory metal film is used for the purposes, among others, of reducing the sheet resistance of the ohmic electrode and permitting metal wiring to be connected to the ohmic electrode without the need for a barrier metal. The metal film may be a **Ni** film or a Co film. The refractory metal film may be a W film, or other film such as Mo film, Ta film, and so on.

Next, as shown in FIG. 4B, a non-single crystal InAs layer 303 is first deposited on the entire surface by a sputtering method using, for example, InAs as the target (for example, magnetron sputtering method), and a **Ni** film 304, WSi film 305 and W film 306 are sequentially deposited by, for example, a sputtering method or an electron beam evaporation method. When a sputtering method such as a magnetron sputtering method is used to make the non-single crystal InAs layer 303, after evacuating the film making

chamber to the base pressure of approximately 2.times.10.sup.-5 Pa, Ar gas up to the pressure of approximately 3.times.10.sup.-1 Pa is introduced to the chamber and DC-discharged. Power consumed for the discharge is, for example, 150 W. The film making temperature is, for example, room temperature. The film making speed is, for example, 7 nm/minute. The thickness of the resist pattern 302 is chosen to be amply larger than the total thickness of the non-single crystal InAs layer 303, **Ni** film 304, WSi film 305 and W film 306.

The n.sup.+ -type GaAs **substrate** 301 now having on it the non-single crystal **InAs** layer 303, **Ni** film 304, WSi film 305 and W film 306 is immersed in organic solvent, such as acetone, to solubly remove the resist pattern 302, hence causing the non-single crystal **InAs** layer 303, **Ni** film 304, WSi film 305 and W film 306 on the resist pattern 302 to be removed together. As a result, as shown in FIG. 4C, only a selective part of the non-single crystal **InAs** layer 303, **Ni** film 304, WSi film 305 and W film 306 in the area corresponding to the opening of the resist pattern 302 remains on the n.sup.+ -type GaAs **substrate** 301.

The n.sup.+ -type GaAs **substrate** 301 having these non-single crystal **InAs** layer 303, **Ni** film 304, WSi film 305 and W film 306, i.e. the multi-layered structure for fabricating the ohmic electrode is then annealed, for example, by a typical electric furnace at, for example, 300.degree. C. for 30 minutes, and subsequently annealed by an RTA (rapid thermal annealing) method or by using a typical electric furnace at, for example, 700 to 800.degree. C. for several seconds to minutes. The melting point of the non-single crystal InAs layer 303

is about 942.degree. C., and that of the n.sup.+ -type GaAs substrate 301 is about 1238.degree. C., which are amply higher than the temperature applied during the annealing. The atmosphere used for the annealing may be composed of N.sub.2 gas with or without an additional small amount of H.sub.2 gas. As a result of the annealing, the ohmic electrode 307 as shown in FIG. 4D is obtained.

Analysis is now being made on details of the structure of the ohmic electrode 307 thus obtained. It has been recognized that part of the ohmic electrode 307 in contact with the n.sup.+ -type GaAs substrate 301 includes n-type crystalline In.sub.x Ga.sub.1-x As and crystalline NiAs. Mechanism of establishment of this structure by the annealing will be explained hereunder. By the first step annealing at, for example, 300.degree. C. for 30 minutes, a Ni.sub.x GaAs layer is made on the n.sup.+ -type GaAs **substrate** 301, and a non-crystalline **InAs** layer containing a precipitate of NiAs is made on the Ni.sub.x GaAs layer. Formation of the Ni.sub.x GaAs layer results in removal of a native oxide film on the n.sup.+ -type GaAs substrate 301. By the second step annealing at, for example, 700 to 800.degree. C. for several seconds or minutes, the non-single crystal **InAs** layer is crystallized due to epitaxial growth on the n.sup.+ -type GaAs **substrate** 301, which results in a crystalline **InAs** layer being made; and the crystalline **InAs** layer subsequently reacts with the n.sup.+ -type GaAs **substrate** 301, which results in the crystalline In.sub.x Ga.sub.1-x As layer being made. The crystalline In.sub.x Ga.sub.1-x As layer and the n.sup.+ -type GaAs substrate 301 are lattice matching at least at a selective portion along the contacting interface between

them. In the second step annealing, Si which is an impurity behaving as a donor is diffused to a high concentration from the WSi film 305 into the crystalline In.sub.x Ga.sub.1-x As layer, and so the crystalline In.sub.x Ga.sub.1-x As layer is changed to an n-type and decreased in resistance. Simultaneously with the formation of the crystalline In.sub.x Ga.sub.1-x As layer, the crystalline NiAs layer is formed on the n.sup.+ -type GaAs substrate 301. Si in the WSi film 305 is diffused also into the n.sup.+ -type GaAs substrate 301 and increases the impurity concentration at least in part of the n.sup.+ -type GaAs substrate 301 in contact with the ohmic electrode 307. It has been recognized that the top portion of the ohmic electrode 307 is composed of W.

FIG. 5 shows measured contact resistances as a function of annealing temperatures, with regard to ohmic electrodes fabricated by using non-single crystal InAs layers 303, WSi films 305 and W films 306 having fixed thicknesses, namely, 18 nm, 4 nm and 50 nm, respectively, and **Ni** films 304 having different thicknesses, namely, 20 nm, 23 nm and 25 nm, and by first depositing the non-single crystal InAs layer 303, **Ni** film 304, WSi film 305 and W film 306, then annealing them at 300.degree. C. for 30 minutes by a method using a typical electric furnace, and finally annealing them at different temperatures ranging from 495.degree. C. to 650.degree. C. for one second by the RTA method. The atmosphere used for the annealing was N.sub.2 gas added with 5% of H.sub.2 gas. n.sup.+ -type GaAs substrates 301 used were prepared by ion implanting Si into (100)-oriented semi-insulating GaAs substrates to change it to an n-type and its impurity concentration is 2.times.10.sup.18

cm.sup.-3. Measurement of contact resistances was conducted by TLM (transmission line method). FIG. 5 describes that the contact resistance is lowest, about 1 .OMEGA.mm, at the annealing temperature of 600.degree. C.

FIG. 6 is an optical micrograph of an aspect just after deposition of the multi-layered structure for fabricating ohmic electrodes composed of the non-single crystal InAs layer 303, **Ni** film 304, WSi film 305 and W film 306 which are 18 nm, 23 nm, 4 nm and 50 nm thick, respectively. FIG. 6 describes that the multi-layered structure for fabricating ohmic electrodes just after the formation has a very good morphology.

FIG. 7 is an optical micrograph of an aspect of the multi-layered structure for fabricating ohmic electrodes composed of the non-single crystal InAs layer 303, **Ni** film 304, WSi film 305 and W film 306 after being annealed at 300.degree. C. for 30 minutes. FIG. 7 describes that the multi-layered structure for fabricating ohmic electrodes at this state also has a very good morphology.

FIG. 8 is an optical micrograph of an aspect of the ohmic electrode for fabricated by first making the multi-layered structure for fabricating ohmic electrodes composed of the non-single crystal InAs layer 303, **Ni** film 304, WSi film 305 and W film 306, then performing the first annealing at 300.degree. C. for 30 minutes and finally performing a subsequent annealing at 650.degree. C. for one second. FIG. 8 describes that the ohmic electrode thus made has quite a good morphology. The reason why such a good morphology is obtained is that the WSi film 305 prevents In of the non-single crystal InAs layer 303 from diffusing toward the electrode surface during the

annealing. It is noteworthy that the WSi film 305, even as quite thin as 4 nm, effectively prevents diffusion of In.

FIG. 9 is an optical micrograph of an ohmic electrode, fabricated, for the purpose of comparison, by first making the multi-layered structure for fabricating ohmic electrodes in which a 23 nm thick non-single crystal InAs layer, 15 nm thick **Ni** film and 34 nm thick W film are sequentially stacked, then annealing the structure at 300.degree. C. for 30 minutes, and finally annealing it at 700.degree. C. for one second. FIG. 9 apparently describes that the ohmic electrode made by this method has a much worse morphology than that of FIG. 8 as a result of diffusion of In from the non-single crystal InAs layer toward the electrode surface.

According to the foregoing first embodiment, since after the multi-layered structure for fabricating ohmic electrodes composing of a non-single crystal **InAs** layer 303, **Ni** film 304, WSi film 305 and W film 306 is made on an n.sup.+ -type GaAs **substrate** 301, the first step annealing at, e.g. 300.degree. C. and the second step annealing at, e.g. 700 to 800.degree. C. are conducted, the ohmic electrode 307 having has a low contact resistance, low film resistance, smooth surface, and good thermal stability. This ohmic electrode 307 has an energy band structure quite similar to the ideal one shown in FIG. 2. In addition, this ohmic electrode 307 permits direct connection of metal wiring without the need for a barrier metal, because its top layer is made of W which is a refractory metal. Furthermore, since the non-single crystal InAs layer 303 used to fabricate the ohmic electrode 307 is made by a sputtering method

which can make a film at a high speed, a high productivity of ohmic electrodes
is promised.

The method for fabricating ohmic electrodes according to the fourth embodiment
uses the multi-layered structure for fabricating ohmic electrodes shown in FIG.
12 in lieu of the one, as shown in FIG. 4C, used in the first embodiment. The
multi-layered structure for fabricating ohmic electrodes shown in FIG. 12 is
different from that of FIG. 4C in not including the WSi film 305 and instead
containing one or more kinds of donor impurities such as Si, Ge Te, Sn, and so
on, in the **Ni** film 304. Accordingly, during the annealing after deposition of
the multi-layered structure for fabricating ohmic electrodes, donor impurities
in the **Ni** film 304 are diffused into the non-single crystal InAs layer 303 and
others. The other aspect of the fourth embodiment is the same as the first
embodiment, and its explanation is omitted.

Next as shown in FIG. 14B, a multi-layered structure composed of the non-single
crystal InAs layer 333 and the **Ni** film 334 is formed on the area for making the
ohmic electrode by the lift-off method as referred to in the explanation of the
first embodiment.

After that, a WSi film is deposited on the entire surface by, for example, a
sputtering method, a resist pattern (not shown) in the form corresponding to
the gate electrode and the ohmic electrode to be made is formed on the WSi film
by a lithography method, the WSi film is etched by, for example, a reactive ion
etching (RIE) method using the resist pattern as a mask and using a CF.sub.4
/O.sub.2 etching gas, and the resist pattern is removed thereafter. As a
result, as shown in FIG. 14C, the structure obtained

includes, on its ohmic electrode making area, multi-layered structures for fabricating ohmic electrodes composed of the non-single crystal InAs layer 333, **Ni** film 334 and WSi film 335, and the gate electrode 341 composed of the WSi film. The WSi film may be used to make wiring.

For example, the **Ni** film 304, 334 used in the first to sixth embodiments may be replaced by a Co film.

10. The multi-layered structure for fabricating an ohmic electrode according to claim 8 wherein said metal film is a **Ni** film or a Co film, and said refractory metal silicide film is a WSi film.

13. The multi-layered structure for fabricating an ohmic electrode according to claim 12 wherein said metal film is a **Ni** film or a Co film, and said refractory metal film is a W film.

15. The multi-layered structure for fabricating an ohmic electrode according to claim 14 wherein said metal film is a **Ni** film or a Co film, and said refractory metal film is a W film.

17. The multi-layered structure for fabricating an ohmic electrode according to claim 14 wherein said metal film is a **Ni** film or a Co film, and said refractory metal film is a W film.